Docket No.: 65744/P018US/10404217
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Blake W. Little et al.

Application No.: 10/821,123 | Confirmation No.: 8209

Filed: April 8, 2004 | Art Unit: 2416

For: SYSTEMS AND METHODS PROVIDING ASICS FOR USE IN MULTIPLE APPLICATIONS | Examiner: P. H. Tran

APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Madam:

As required under 37 C.F.R. § 41.37(a), this Brief and Petition for Extension of time are filed within three months of the Notice of Appeal filed in this case on January 23, 2009 and are in furtherance of said Notice of Appeal.

The fees required under 37 C.F.R. § 41.20(b)(2) are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1205:

VIII. Claims Appendix
IX. Evidence Appendix
X. Related Proceedings Appendix

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is:

Sonosite, Inc.

II. RELATED APPEALS, INTERFERENCES, AND JUDICIAL PROCEEDINGS

There are no other appeals, interferences, or judicial proceedings, which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 34 claims pending in application.

B. Current Status of Claims

1. Claims canceled: 0

2. Claims withdrawn from consideration but not canceled: 0

3. Claims pending: 1-34

4. Claims allowed: 0

5. Claims rejected: 1-34

C. Claims On Appeal

The claims on appeal are claims 1-34

IV. STATUS OF AMENDMENTS

Appellant filed an Amendment After Final Rejection on March 10, 2009 and received an Advisory Action mailed March 23, 2009.

V. SUMMARY OF CLAIMED SUBJECT MATTER

For the convenience of the Board and pursuant to M.P.E.P. 1205 (c)(v), Appellant has included, by way of example, a concise explanation of the subject matter defined in each of the independent claims and many of the dependent claims. To ensure brevity, the explanatory examples cite to only one exemplary embodiment. Other passages not cited herein may provide additional explanation of the subject matter.

An embodiment of the present invention is described in claim 1 which includes a system comprising an application specific integrated circuit (ASIC) 102 of Figure 1 adapted for use in a plurality of systems as described in paragraph [0020] of the originally filed application. Wherein the system is one of the plurality of systems, and each system has a circuit configuration that uses a different number of signal channels for further processing by the application specific integrated circuit as described in paragraph [0021] of the originally filed application.

An embodiment of the present invention is described in claim 2 which includes the system of claim 1 wherein the ASIC comprises a plurality of multiplexors providing N to M signal multiplexing, wherein in a first configuration of the circuit configurations the ASIC is configured to provide N to M signal multiplexing, and wherein in a second configuration of the circuit configuration the ASIC is configured to provide N to M/2 signal multiplexing as described in paragraphs [0021] and [0030] of the originally filed application.

outputs, at least one select signal input, and at least one enable signal input, the enable signal input being utilized in providing the N to M/2 signal multiplexing of the second configuration as described in paragraphs [0021] and [0030] of the originally filed application.

An embodiment of the present invention is described in claim 10 which includes a system comprising an application specific integrated circuit (ASIC) 210 of Figure 2A adapted for use in a plurality of circuit configurations as described in paragraph [0024] of the originally filed application. Further, the circuit configurations provide for different numbers of signal channels for further processing using same circuitry of the application specific integrated circuit as described in paragraph [0021] of the originally filed application. Moreover, the ASIC 210 is included in an application comprising a transducer 201 of Figure 2A, a beam former 221, and a data path 104 of Figure 1, and wherein the data path is in communication with the ASIC, the transducer, and the beam former as explained in paragraph [0020] and figure 1 of the originally filed application.

An embodiment of the present invention is described in claim 11 which includes the system of claim 10 wherein the application further comprises a signal processing unit external to the data path and in communication with the data path at a number of points thereon and is operable to capture and insert information in the data path at each of those number of points as explained in paragraph [0020] and figure 1 of the originally filed application.

An embodiment of the present invention is described in claim 12 which includes a method comprising determining a number of channels for use in a data path 801 of Figure 8 and configuring an ASIC adapted for use in a plurality of systems 802 of Figure 8 as explained in paragraph [0006] of the originally filed application. Further, each system has a circuit configuration that uses a different number of channels, to provide the determined number of channels as explained in paragraph [0007] of the originally filed application.

An embodiment of the present invention is described in claim 13 which includes a method comprising determining a number of channels for use in a data path and configuring an ASIC adapted for use in a plurality of configurations to provide the determined number of

channels as explained in figure 8 and paragraph [0051] of the originally filed application. Further, the method comprises implementing in a sonogram imaging system the ASIC, a first beam former, the data path, and a transducer array, wherein the ASIC, the first beam former, and the transducer array are in communication with the data path as explained in paragraph [0051]. See, figure 8 and paragraph [0051] of the originally filed application.

An embodiment of the present invention is described in claim 14 which includes the method of claim 12 further comprising summing data on each of at least two channels by the ASIC as described in paragraph [0032] of the originally filed application.

An embodiment of the present invention is described in claim 24 which includes the method of claim 12 further comprising implementing a signal processing unit to communicate with the data path at a number of points as shown in paragraph [0020] of the originally filed application. Furthermore, the method includes programming the signal processing unit with code to provide a mode of functionality not originally included in a platform and operating the signal processing unit to intercept and insert data along the number of points on the path, thereby instructing the platform to perform the mode as shown in paragraph [0048] of the originally filed application.

An embodiment of the present invention is described in claim 25 which includes an apparatus comprising a sonogram imaging system including a transducer 201 of Figure 2A, a beam former 221 of Figure 2A, a data path including a plurality of information channels connecting the transducer to the beam former, and an ASIC 210 of Figure 2A in communication with the data path between the transducer and the beam former, including circuitry operable as a bank of multiplexors to decrease a number of the information channels from the transducer to the beam former as disclosed in Figure 2A of the originally filed application.

An embodiment of the present invention is described in claim 29 which includes an apparatus comprising a sonogram imaging system including a transducer 401, a beam former 431, a data path including a plurality of information channels connecting the transducer to the beam former, and an ASIC 410 in communication with the data path between the transducer and

the beam former, including circuitry operable as a summer/cross-point switch, to route a number of information channels from the transducer to the beam former as disclosed in paragraphs [0041] and [0042] of the present application.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Claims 2-5 stand rejected under 35 U.S.C. § 112, first paragraph.

B. Claims 1-24 stand rejected under 35 U.S.C. § 112, second paragraph.

C. Claims 1-3, 10-14, and 24 stand rejected under 35 U.S.C. § 102(b) as being anticipated by *Snyder* (United State Patent Number 5,520,187).

D. Claims 25-29 and 32-33 stand rejected under 35 U.S.C. § 102(b) as being anticipated by *Knell* et al. (United States Patent Number 6,468,213).

E. Claims 4-9 and 15-21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Snyder* in view of *Agelsen et al.* (United States Publication 2005/023402).

F. Claims 22-23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Snyder* in view of *Knell*.

G. Claims 30, 31, and 34 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Knell* in view of *Kristoffersen* (United States Publication 2005/0113698).

VII. ARGUMENT

Each of the rejections are traversed herein. The claims do not stand or fall together.

A. Rejection under 35 U.S.C. § 112, first paragraph – First Ground of Rejection

Claims 2-5 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. Specifically, the *Office Action* states that the limitations N to M/2 multiplexing are not disclosed in the specification.

Appellant notes that the phrase "N to M/2", as appears in claims 2-5 does not appear word-for-word in the specification. However, "[t]he subject matter of the claim need not be described literally (i.e., using the same terms or *in haec verba*) in order for the disclosure to satisfy the description requirement." See M.P.E.P. § 2163.02. One skilled in the art would recognize that given a variable "M", the "M/2" is one half of M. Furthermore, Appellant asserts that the specification's discussion of 2:1 multiplexers and 4:1 multiplexers appearing paragraphs [0021] and [0030], is sufficient to clearly convey to one of ordinary skill in the art the invention that is claimed. Thus, Appellant respectfully requests the rejection of claims 2-5 under 35 U.S.C. § 112, first paragraph be reversed.

B. Rejections Under 35 U.S.C. § 112, second paragraph – Second Ground of Rejection

Claims 1-24 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Appellant regards as the invention. Specifically, the *Office Action* states independent claims 1, 10, 12, and 13 include the phrase "adapted for" making it unclear whether the limitations following the phrase are part of the claimed invention. *Office Action* at 6. Further, dependent claims 2-9, 11, and 14-24 stand rejected because they depend from rejected claims 1, 10, and 12. See *Office Action* at 6.

There has been much confusion surrounding this rejection since the Office Action of November 13, 2008. Specifically, after receiving this § 112 rejection, Lisa Joni Collins (Applicant's Attorney registration number 59,354) and Examiner Maxwell Clark conducted a telephonic Examiner Interview on January 22, 2009 and discussed this § 112 rejection of claims 1, 10, 12, and 13 (and the claims depending therefrom). The discussion centered around the holding of *Hopper v. Microsoft*, 405 F.3d 1326, 1329 74 USPQ2d 1481, 1483 (Fed. Cir. 2005) which explains that when a clause states a condition that is material to patentability, it cannot be ignored. See also M.P.E.P. § 2111.04. It was agreed that because the limitations following the phrase "adapted for" are material to patentability, the limitations cannot be ignored. Thus, the

limitations following the phrase should be read as part of the claimed invention. Since the limitation should be read as part of the claim, it should be clear that the limitations following the phrase "adapted for" are part of the claimed invention. As such, the claims particularly point out the subject matter which Appellant regards as the invention.

At the conclusion of the January 22, 2009 Examiner Interview, the Examiner and Appellant were in agreement, and Appellant was expecting an advisory action withdrawing the rejection such that the issues on appeal would be narrowed. However, rather than sending an advisory action withdrawing the rejection, Examiner Clark sent an Interview Summary dated January 30, 2009 indicating that he wanted the Appellant to file a Response After Final discussing *Hopper* and M.P.E.P. § 2111.04 so that he could withdraw the rejection as agreed.

Attorney Collins attempted to contact Examiner Clark to remedy the misunderstanding; however, her attempts were unsuccessful because Examiner Clark left his position with the Patent and Trademark Office and the application was reassigned to Examiner Phuc H. Tran.

Once Examiner Tran received the file, Attorney Collins and Examiner Tran conducted a telephonic Examiner Interview on March 3, 2009 discussing this § 112 rejection. Examiner Tran requested that Attorney Collins file a response after final discussing *Hopper* and M.P.E.P. § 2111.04, and Attorney Collins complied by filing a Response After Final on March 10, 2009. Appellant again expected an advisory action withdrawing the rejection such that the issues on appeal would be narrowed. However, rather than sending an advisory action withdrawing the rejection and narrowing the issues, Examiner Tran sent the Advisory Action dated March 23, 2009 indicating he focused on the § 112 rejection of claims 2-5 rather than the § 112 rejection based on the phrase "adapted for" discussed in the Examiner Interview. Examiner Tran made no mention at all of the discussed § 112 rejection in the Advisory Action. As such, much confusion has surrounded this 35 U.S.C. § 112 rejection, and it is unclear to Appellant whether the rejection has been withdrawn. Nevertheless, in the interest of caution, Appellant presents arguments showing that this rejection should be reversed.

Regarding the appropriateness of the 35 U.S.C. § 112 rejection, *Hopper v. Microsoft*, 405 F.3d 1326, 1329 74 USPQ2d 1481, 1483 (Fed. Cir. 2005) holds that when a clause states a condition that is material to patentability, it cannot be ignored. See also M.P.E.P. § 2111.04. Because the limitations following the phrase "adapted for" are material to patentability, the limitations cannot be ignored. Thus, the limitations following the phrase should be read as part of the claimed invention. Since the limitation should be read as part of the claim, it should be clear that the limitations following the phrase "adapted for" is part of the claimed invention. As such, the claims particularly point out the subject matter which Appellant regards as the invention, and Appellant requests the Board reverse the rejection.

C. Rejections Under 35 U.S.C. § 102 – Third Ground of Rejection

Claims 1-3, 10-14, and 24 stand rejected under 35 U.S.C. § 102(b) as being anticipated by *Snyder*.

It is well settled that to anticipate a claim, the reference must teach every element of the claim, see M.P.E.P. § 2131. Furthermore, in order for a prior art reference to be anticipatory under 35 U.S.C. § 102 with respect to a claim, "[t]he identical invention must be shown in as complete detail as is contained in the . . . claim," see M.P.E.P. § 2131, citing Richardson v. Suzuki Motor Co., 9 U.S.P.Q.2d 1913 (Fed. Cir. 1989). Appellant respectfully asserts that because the references do not teach each element of the claims, the claims are not anticipated.

1. Claim 1

Claim 1 recites in part " [a] system comprising: an application specific integrated circuit (ASIC) . . . ." The *Office Action* cites the Abstract of *Snyder* as teaching an ASIC. *Office Action* at 6. However, *Snyder* does not teach the ASIC of claim 1. Rather, *Snyder* discloses a programmable probe multiplexer which is a field programmable gate array (FPGA). *Snyder* at column 5, lines 27-28 and Figures 3 and 4. Because *Snyder* fails to teach "[a] system comprising: an application specific integrated circuit (ASIC)," *Snyder* fails to anticipate claim 1. Thus, Appellant requests the Board reverse the rejection of record.

2. Claims 2-3

Claims 2-3 depend from independent claim 1 thereby inheriting all the claim limitations of claim 1. As explained above, *Snyder* fails to teach each of the limitations of claim 1; thus, at least due to its dependence from claim 1, claims 2-3 contain limitations not taught by *Snyder*. Therefore, *Snyder* does not anticipate claims 2-3, and Appellant requests the Board reverse the rejections.

3. Claim 10

Claim 10 recites in part "[a] system comprising: an application specific integrated circuit (ASIC) . . . ." The *Office Action* cites the Abstract of *Snyder* as teaching an ASIC. *Office Action* at 7. However, *Snyder* does not teach the ASIC of claim 10. Rather, *Snyder* discloses a programmable probe multiplexer which is a field programmable gate array (FPGA). *Snyder* at column 5, lines 27-28 and Figures 3 and 4. Because *Snyder* fails to teach "[a] system comprising: an application specific integrated circuit (ASIC)," *Snyder* fails to anticipate claim 10. Thus, Appellant requests the Board reverse the rejection of record.

4. Claim 11

Claim 11 depends from independent claim 10 thereby inheriting all the claim limitations of claim 10. As explained above, *Snyder* fails to teach each of the limitations of claim 10; thus, at least due to its dependence from claim 10, claim 11 contains limitations not taught by *Snyder*. Therefore, *Snyder* does not anticipate claim 11, and Appellant requests the Board reverse the rejection.

5. Claim 12

Claim 12 recites in part "configuring an ASIC . . . ." The *Office Action* cites column 2, lines 50-52 of *Snyder* as teaching the claim's limitation. *Office Action* at 8. However, *Snyder* does not teach configuring an ASIC. Rather, *Snyder* discloses reconfiguration of a programmable probe multiplexer which is a field programmable gate array (FPGA). *Snyder* at

column 5, lines 27-28 and Figures 3 and 4. Because *Snyder* fails to teach "configuring an ASIC," *Snyder* fails to anticipate claim 12. Thus, Appellant requests the Board reverse the rejection of record.

6. Claim 13

Claim 13 recites in part "configuring an ASIC ... and implementing ... the ASIC . . . ." The *Office Action* cites column 2, lines 50-52 of *Snyder* as teaching the claim's limitation. *Office Action* at 9. However, *Snyder* does not teach configuring an ASIC or implementing the ASIC. Rather, *Snyder* discloses reconfiguration of a programmable probe multiplexer which is a field programmable gate array (FPGA). *Snyder* at column 5, lines 27-28 and Figures 3 and 4. Because *Snyder* fails to teach "configuring an ASIC ... and implementing ... the ASIC," *Snyder* fails to anticipate claim 13. Thus, Appellant requests the Board reverse the rejection of record.

7. Claim 14

Claim 14 recites in part "summing data on each of at least two channels by the ASIC." The *Office Action* cites column 2, lines 9-10 of *Snyder* as teaching summing data by the ASIC. *Office Action* at 9. However, the cited portion of *Snyder* teaches ***beamformer*** 2 outputs two summed beams. In the rejection, the Appellee likens *Snyder's* programmable multiplexer (not beamformer) to the claims' ASIC. Thus, regardless of whether *Snyder's* beamformer 2 sums beams, based the Appellee's reading of *Snyder* on the claim, *Snyder* does not teach summing data ***by the ASIC***. Accordingly, the Appellee fails to make a prima facie showing of anticipation; thus, Appellant requests the Board reverse the rejection. Moreover, claim 14 requires an ASIC. As explained above, *Snyder* fails to teach the required ASIC. Rather, *Snyder's* teachings disclose an FPGA. Therefore, claim 14 is not anticipated by *Snyder*, and Appellant requests the Board reverse the rejection.

8. Claim 24

Claim 24 recites in part "programming the signal processing unit with code to provide a mode of functionality not originally included in a platform using the method . . . ." The *Office Action* cites column 2, lines 3-4 of *Snyder* as teaching this limitation. *Office Action* at 9-10. However, the cited portion of *Snyder* fails to teach programming with code to provide a mode of functionality not originally included in a platform. Rather, *Snyder* teaches programming with synchronization ***options*** suggesting *Snyder's* programming may be limited to the ***options*** originally included in his platform. Because *Snyder's* programming appears to be limited to options originally included in his platform, *Snyder* does not teach programming the unit with code not originally included in the platform. *Snyder* at col. 2, lines 3-5. Moreover, claim 24 depends from independent claim 12 thereby inheriting all of claim 12's limitations. Thus, because claim 12 is not taught but *Snyder*, as explained above, *Snyder* fails to teach each limitation of claim 24. Accordingly, because *Snyder* does not teach each and every limitation of claim 24, Appellant requests the Board reverse the rejection of record.

D. Rejections Under 35 U.S.C. §102(b) – Fourth Ground of Rejection

Claims 25-29 and 32-33 stand rejected under 35 U.S.C. § 102(b) as being anticipated by *Knell* et al.

1. Claim 25

Claim 25 defines an apparatus that includes an ASIC in communication with the data path between the transducer and the beam former, including circuitry operable as a bank of multiplexers to decrease a number of the information channels from the transducer to the beam former. *Knell* does not disclose these limitations. *Knell* mentions that a derotation multiplexer may be used. *Knell* at col. 18, lines 44-45. The Examiner then takes notice that because there is a multiplexer, then the number of information channels is decreased. *Office Action* at 10-11. Appellant notes that the cited multiplexer of *Knell* is a derotation multiplexer that is used to handle a linear or curved transducer. *Knell* does not disclose that the multiplexer needs to reduce

the channels to address the linear or curved transducer. The other portions of *Knell* cited to support the assertion of the *Office Action* also do not provide the necessary teaching. Column 18, lines 26-45 discusses using timing delay devices and the derotation multiplexer. Column 13, lines 25-32 discusses delaying signals of different channels. Column 13, lines 42-45 discusses connecting inputs with outputs. Nothing in *Knell*, even with the supplement of official notice, teaches the limitations of the claim. Thus, *Knell* does not teach all of the claimed limitations, and the elements are not arranged in the same manner as the claim. Therefore, the Appellant respectfully asserts that for the above reasons claim 25 is patentable over the 35 U.S.C. § 102 rejection of record and requests the Board allow the claim.

2. Claim 29

Claim 29 defines an apparatus that includes an ASIC in communication with the data path between the transducer and the beam former, including circuitry operable as a summer/cross-point switch, to route a number of information channels from the transducer to the beam former. *Knell* does not disclose both a summer ***and*** a cross-point switch as required by the claim. Moreover, the Examiner appears to agree because in rejecting claim 30, the Examiner states that *Knell* does not disclose a cross-point circuitry, see page 20, line 8 of the *Office Action.* Thus, *Knell* does not teach all of the claimed limitations, and the elements are not arranged in the same manner as the claim. Therefore, the Appellant respectfully asserts that for the above reasons claim 29 is patentable over the 35 U.S.C. § 102 rejection of record. Appellant respectfully requests the Board reverse the rejection.

3. Claims 26-28

Claims 26-28 depend from base claim 25, and thus inherit all limitations of claim 25. Each of claims 26-28 sets forth features and limitations not recited by *Knell*. Thus, the Appellant respectfully asserts that for the above reasons claims 25-29 are patentable over the 35 U.S.C. § 102 rejection of record.

4. Claims 32-33

Claims 32-33 depend from base claim 29, and thus inherit all limitations of claim 29. Each of claims 32-33 sets forth features and limitations not recited by *Knell*. Thus, the Appellant respectfully asserts that for the above reasons claims 32-33 are patentable over the 35 U.S.C. § 102 rejection of record.

E. Rejections Under 35 U.S.C. § 103 of Claims 4-9 and 15-21 – Fifth Ground of Rejection

The test for nonobvious subject matter is whether the differences between the subject matter and the prior art are such that the claimed subject matter as a whole would have been obvious to a person having ordinary skill in the art to which the subject matter pertains. The United States Supreme Court in Graham v. John Deere and Co., 383 U.S. 1 (1966) set forth the factual inquiries which must be considered in applying the statutory test: (1) determining of the scope and content of the prior art; (2) ascertaining the differences between the prior art and the claims at issue; (3) resolving the level of ordinary skill in the pertinent art, and (4) evaluate evidence of secondary considerations. The current USPTO Guidelines incorporate the mandate of Graham and directs the Examiner to set forth in the *Office Action* the resolution of the factual inquires of Graham and provide a rationale to support the rejection. The rejection must address all of the limitations of the claims.

Claims 4-9 and 15-21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Snyder* in view of *Agelsen et al.*

Base claims 1 and 12 are defined as described above. *Snyder* does not teach all limitations of claims 1 and 12 as described above. *Angelsen* is not relied upon as disclosing the limitations deficient from *Snyder*. Therefore, the combination *Snyder* and *Angelsen* does not teach all elements of the claimed invention.

Claims 4-9 and 15-21 depend from base claims 1 and 12, and thus inherit all limitations of claims 1 and 12. Each of claims 4-9 and 15-21 sets forth features and limitations not recited

by the combination of *Snyder* and *Knell*. Thus, the Appellant respectfully asserts that for the above reasons claims 4-9 and 15-21 are patentable over the 35 U.S.C. § 103(a) rejections of record. Thus, Appellant requests the Board reverse the rejections.

F. Rejections Under 35 U.S.C. § 103(a) of Claims 22-23 – Sixth Ground of Rejection

Claims 22-23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Snyder* in view of *Knell*.

Claims 22-23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Snyder* in view of *Knell*. Base claim 12 is defined as described above. *Snyder* does not teach all limitations of claim 12 as described above. *Knell* is not relied upon as disclosing the limitations deficient from *Snyder*. Therefore, the combination *Snyder* and *Knell* does not teach all elements of the claimed invention.

Claims 22-23 depend from base claim 12, and thus inherit all limitations of claim 12. Each of claims 22-23 sets forth features and limitations not recited by the combination of *Snyder* and *Knell*. Thus, the Appellant respectfully asserts that for the above reasons claims 22-23 and 34 are patentable over the 35 U.S.C. § 103(a) rejection of record. Thus, Appellant requests the Board reverse the rejections.

G. Rejections Under 35 U.S.C. §103(a) of Claims 30, 31, and 34 – Seventh Ground of Rejection

Claims 30, 31, and 34 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Knell* in view of *Kristoffersen*.

Claims 30, 31, and 34 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Knell* in view of *Kristoffersen*. Base claim 29 is defined as described above. *Knell* does not teach all limitations of claim 29 as described above. *Kristoffersen* is not relied upon as

disclosing the limitations deficient from *Knell*. Therefore, the combination *Knell* and *Kristoffersen* does not teach all elements of the claimed invention.

Claims 30-31 and 34 depend from base claim 29, and thus inherit all limitations of claim 29. Each of claims 30-31 and 34 sets forth features and limitations not recited by the combination of *Knell* and *Kristoffersen*. Thus, the Appellant respectfully asserts that for the above reasons claims 30-31 and 34 are patentable over the 35 U.S.C. § 103(a) rejection of record. Thus, Appellant requests the Board reverse the rejections.

VIII. CLAIMS APPENDIX

A copy of the claims involved in the present appeal is attached hereto as Appendix A.

IX. EVIDENCE APPENDIX

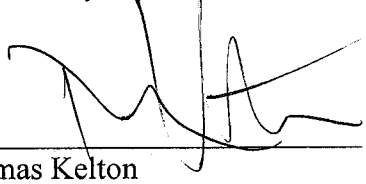
No evidence pursuant to §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the examiner is being submitted.

X. RELATED PROCEEDINGS APPENDIX

No related proceedings are referenced in II. above, hence copies of decisions in related proceedings are not provided.

Dated: April 9, 2009

Respectfully submitted,



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Appeal Brief

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being transmitted via the Office electronic filing system in accordance with § 1.6(a)(4).

Dated: April 9, 2009

Signature: _____
(Joy H. Perigo)

APPENDIX A

1. A system comprising:

an application specific integrated circuit (ASIC) adapted for use in a plurality of systems, wherein the system is one of the plurality of systems, and each system has a circuit configuration that uses a different number of signal channels for further processing by said application specific integrated circuit.

2. The system of claim 1, wherein said ASIC comprises:

a plurality of multiplexors providing N to M signal multiplexing, wherein in a first configuration of said circuit configurations said ASIC is configured to provide N to M signal multiplexing, and wherein in a second configuration of said circuit configuration said ASIC is configured to provide N to M/2 signal multiplexing.

3. The system of claim 2, wherein said plurality of multiplexors include N signal inputs, M signal outputs, at least one select signal input, and at least one enable signal input, said enable signal input being utilized in providing said N to M/2 signal multiplexing of said second configuration.

4. The system of claim 3, wherein said plurality of multiplexors are divided into hardwired pairs, and only one of each pair is enabled during a receive operation.

5. The system of claim 3, wherein at least one of said select signal input and said enable signal input comprise a digital serial control bus.

6. The system of claim 1, wherein said ASIC comprises:

a circuit configurable to provide a cross point switch function in a first configuration of said circuit configurations and to provide a signal summer function in a second configuration of said circuit configurations.

7. The system of claim 6, wherein said cross-point switch function comprises selectively routing signal channels to one or more beam formers.

8. The system of claim 6, wherein the signal summer function comprises a symmetric signal summing operation.

9. The system of claim 8, wherein the symmetric signal summing operation comprises summing one or more signals that are determined to be of similar weight and delay.

10. A system comprising:

an application specific integrated circuit (ASIC) adapted for use in a plurality of circuit configurations, said circuit configurations providing for different numbers of signal channels for further processing using same circuitry of said application specific integrated circuit;

wherein the ASIC is included in an application comprising a transducer, a beam former, and a data path, and wherein the data path is in communication with the ASIC, the transducer, and the beam former.

11. The system of claim 10, wherein the application further comprises a signal processing unit external to the data path and in communication with the data path at a number of points thereon and is operable to capture and insert information in the data path at each of those number of points.

12. A method comprising:

determining a number of channels for use in a data path; and

configuring an ASIC adapted for use in a plurality of systems, wherein each system has a circuit configuration that uses a different number of channels, to provide said determined number of channels.

13. A method comprising:

determining a number of channels for use in a data path;

configuring an ASIC adapted for use in a plurality of configurations to provide said determined number of channels; and

implementing in a sonogram imaging system the ASIC, a first beam former, the data path, and a transducer array, wherein the ASIC, the first beam former, and the transducer array are in communication with the data path.

14. The method of claim 12 further comprising summing data on each of at least two channels by the ASIC.

15. The method of claim 14, wherein summing data comprises:

receiving signals from a control circuit instructing that certain of the channels are to be divided into symmetric pairs and those pairs added, thereby decreasing the number of output channels; and

routing the added pairs to one or more beam formers.

16. The method of claim 14, wherein summing data comprises:

receiving signals from a control circuit instructing that certain of the channels are to be divided into adjacent pairs and those pairs added, thereby decreasing the number of output channels; and

routing the added pairs to one or more beam formers.

17. The method of claim 12 further comprising operating circuitry on the ASIC as a cross-point switch to increase the number of channels from the ASIC to one or more beam formers.

18. The method of claim 17, wherein operating as a cross-point switch comprises receiving signals from a control circuit instructing that certain of the channels be routed to one or more of the beam formers.

19. The method of claim 12 further comprising operating circuitry on the ASIC as a plurality of multiplexors, thereby decreasing the number of channels from a transducer array to a beam former.

20. The method of claim 19, wherein the multiplexors are 2:1 multiplexors, and wherein operating as a plurality of multiplexors comprises selectively enabling one of every two 2:1 multiplexors, thereby providing 4:1 multiplexing functionality.

21. The method of claim 20, wherein selectively enabling comprises stimulating an enable switch on one of every two 2:1 multiplexors by a control signal from a beam former.

22. The method of claim 12 further comprising implementing two beam formers in communication with the data path; and

operating the two beam formers and a transducer array to form multiple receive beams.

23. The method of claim 22 further comprising operating the two beam formers and the transducer array perform a multi-line receive operation.

24. The method of claim 12 further comprising implementing a signal processing unit to communicate with the data path at a number of points;

programming the signal processing unit with code to provide a mode of functionality not originally included in a platform using the method; and

operating the signal processing unit to intercept and insert data along the number of points on the path, thereby instructing the platform to perform the mode.

25. An apparatus comprising:

a sonogram imaging system including:

a transducer;

a beam former;

a data path including a plurality of information channels connecting the transducer to the beam former; and

an ASIC in communication with the data path between the transducer and the beam former, including circuitry operable as a bank of multiplexors to decrease a number of the information channels from the transducer to the beam former.

26. The apparatus of claim 25, wherein the circuitry on the ASIC comprises a plurality of 2:1 multiplexors, wherein each mutliplexor includes an enable switch and a select switch.

27. The apparatus of claim 26, wherein the beam former controls the enable and select switches on each of the plurality of 2:1 multiplexors to provide a higher-order multiplexing functionality.

28. The apparatus of claim 27 further comprising a digital serial control bus to connect the enable and select switches to the beam former.

29. An apparatus comprising:

a sonogram imaging system including:

a transducer;

a beam former;

a data path including a plurality of information channels connecting the transducer to the beam former; and

an ASIC in communication with the data path between the transducer and the beam former, including circuitry operable as a summer/cross-point switch, to route a number of information channels from the transducer to the beam former.

30. The apparatus of claim 29, wherein the circuitry included by the ASIC comprises a summation bus and cross-point switch circuitry.

31. The apparatus of claim 30, wherein the summation bus is operable to decrease a number of information channels between the transducer and the beam former.

32. The apparatus of claim 29, wherein the circuitry included by the ASIC is controlled by the beam former via a bus.

33. The apparatus of claim 32, wherein the beam former sends instructions to logic included in the ASIC via the bus to process data as a summer.

34. The apparatus of claim 32, wherein the beam former sends instructions to logic included in the ASIC via the bus to process data as a cross-point switch.

APPENDIX B

No evidence pursuant to §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the examiner is being submitted.

APPENDIX C

No related proceedings are referenced in II. above, hence copies of decisions in related proceedings are not provided.